Written by Marco Attard
10 November 2010

Intel, Toshiba and Samsung will team up to develop technologies to reduce NAND flash memory circuitry sizes to nearly 10nm by 2016.

Current flash chips are 20nm in size.

The 3 companies intend to form a consortium with around 10 other semiconductor companies.

Toshiba and Samsung will use the technologies to make more dense NAND flash chips, and Intell will use it to develop faster microprocessors.

The Nikkei daily reports Japan's ministry of economy, trade and industry will likely provide 5 billion ($61 million) of the roughly 10 billion yen ($122 million) in initial funds for R&D.

Go Report: Intel, Samsung and Toshiba Join Hands to Halve Chip Size (Reuters)