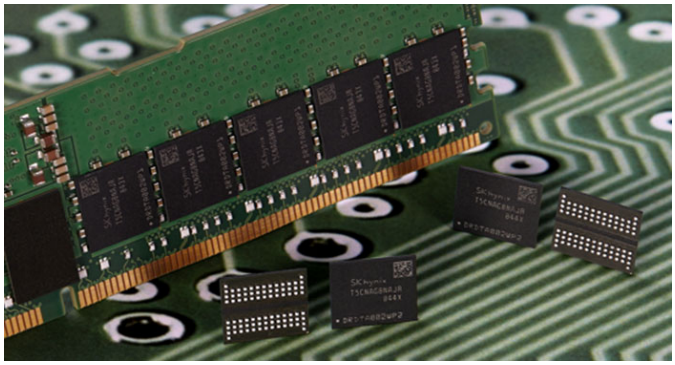
SK Hynix provides technical details of the upcoming DDR5-6400 memory chip at the International Solid State Circuits Conference-- a 16Gb device (organised in 32 banks and 8 bank groups) built using a 2nd-gen 10nm fabrication technology with four metal layers.



As detailed by EETimes, the chip runs at 1.1V and measures 76.22mm2. The presentation had the company describe the challenges of making the chip, such as the implementation of a modified delay-locked loop (DLL) using phase rotator and an injection locked oscillator to reduce the clock jitter and clock duty cycle distortion associated with operating at higher clock speeds.

Back in November 2018 SK Hynix claimed to have developed a first DDR5 DRAM chip meeting JEDEC standards, even if the standard wasn't actually set in stone at the time. In fact the JEDEC LPDDR5 standard remains a work in progress, although last week the organisation announced the chips will run at an I/O rate of 6400 MT/s, 50% higher than the first version of LPDDR4.

Go Hynix Details First DDR5 Chip (EETimes)